PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	OCuLink BP Type Rev 1.7
DATE:	January 6, 2017
AFFECTED DOCUMENT:	OCuLink Specification version 1.0
SPONSOR:	Jay Neer (Molex), Alex Haser (Molex)

Part I

1. Summary of the Functional Changes

The backplane type (BP Type) signal was incompletely specified. Table 2-2 did not include a Type of logic used for this signal. No definition is provided for the logic levels of this signal.

2. Benefits as a Result of the Changes

Specifying the functionality of the BP Type sideband allows designs to interoperate. Add the ability for this signal to be used for vendor specific purposes after it intitially derermins the interface type.

3. Assessment of the Impact

The BP Type sideband is implementable.

4. Analysis of the Hardware Implications

Specification provided that is necessary for hardware to be designed.

5. Analysis of the Software Implications

No impact on software.

6. Analysis of the C&I Test Implications

No impact on testing.

NOTE: This ECR is to be submitted for review at the same time as the CPRSNT ECR. These documents complement each other and both are necessary to fully understand the proposed changes.

Part II

Detailed Description of the change

Change Sections 2.3 and 2.4 as follows (see next page):

2.3 Signal Description

Upstream/ downstream port assignment is defined as shown in Figure 2-x below. This naming convention is consistent across all PCIe documentation. Refer to the Base Specification for more information.

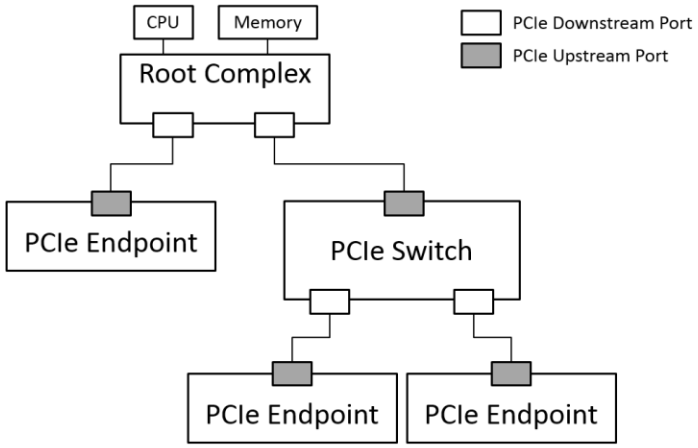

Figure 2-x. Upstream/ downstream port assignment

Table 0-1. Signal Description

Leave remaining content in this section as is.

2.4. Signal Compatibility Matrix

- All auxiliary signals are required from a cabling perspective.
- The signals listed in Table 2-2 are for an Upstream and/or Downstream Subsystem, with a brief description of features enabled by it.

Table 2-2. Signal Compatibility Matrix

Signal	Type	~~Root / Downstream Subsystem~~Upstream Subsystem	Cable Assembly	~~End Point / Upstream Subsystem~~Downstream Subsystem	Comments
CPRSNT#	3.3 V Logic	Required Output	Required	Required Input	Required on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Possible states: High (3.3 V) and (3.3 V)/2.
CWAKE#/ (OBFF) (Note 1)	3.3 V Logic	Optional Input/ (Optional I/O)	Required	Optional Output/ (Optional I/O)	Optional on both sides of the cable. The driver is open-drain type and requires high impedance during power off states. Signal becomes bidirectional if both ends support OBFF.
PERST#	3.3 V Logic	Required ~~Output~~Input	Required	Required ~~Input~~Output	When negated indicates when the applied main power is within the specified tolerance and is stable. (Cable installed and power not applied).
VSP	User defined	Optional I/O	Required (Notes ~~1,~~2, 3, 4, 5)	Optional I/O	Optional on both sides of the cable, function specified by vendor, is permitted to be used to support legacy functions or future functionality.
BP TYPE / (VSP) (Note 1)	3.3 V Logic	Optional Out~~In~~put/ (Optional I/O)	Required (Note 6~~5~~)	O~~O~~ptional In~~Out~~put/ (Optional I/O)	Input required to enable a full crossover internal cable solution.

Notes:

1. The first signal type listed is required to support OCuLink functionality; the associated Upstream/ Downstream assignments for this signal type are listed first in their respective columns. The second signal type, listed in parentheses, is an optional implementation; Upstream / Downstream assignments associated with these options are also listed second, in parentheses, in their respective columns.
2. The SMBus/ 2-Wire interface employed in this specification can be a Passive or Active implementation. The Passive solution may provide a connection from the root to the endpoint to a) determine its usage or b) for device management. Due to complexity, Active Optical Cables may not want to implement this option and are permitted to have a reduced feature set. Requirements for PCI Express cables with reduced feature sets are described in SFF-8449.

~~1. The use of SMBus across the cable is an optional feature. This allows the use of cables that adhere to SFF-8449 for a PCI Express interface with a reduced feature set. Active Optical Cable assemblies may not want to implement SMBus across the cable for cost or complexity reasons, and therefore is permitted to have a reduced feature set. The Upstream Subsystems should not be designed in such a way as to require the use of SMBus across the cable. However, the SMBus controller is still required by both Upstream and Downstream fixed ends to read the cable assembly information for configuration of the PCIe devices that are part of the cabled Link.~~

~~2.~~3. It is recommended that systems employing VSP for REFCLK functionality utilize pins A12+/A13- for the ROOT and pins B12+/B13- for the ENDPOINT.

~~3.~~4. SRIS architecture on Upstream and Downstream Subsystems is required if supporting no-wire VSP positions between Upstream and Downstream Subsystems

~~4.~~ Verify systems enabling unshielded wire at VSP positions meet EMI emission and EMI susceptibility limits, as required by target market regulatory bodies.

5.

6. Refer to SFF-8448 for signaling details (Other 2-Wire Type). Once the Backplane Type has been determined, it does not preclude the Controller/ Root from using this signal for some other user/vendor specific defined application.

~~Logic levels 0 and 1 are based on CMOS 3.3 V logic VIL<0.3 × VCC, VIH>0.7 × VCC. The high signaling level indicates 2-wire interface. A low signal level indictes SGPIO (refer to SFF-8448). The Endpoint must have a 4.7 kΩ resistor with a relative tolerance of 5% connected to VCC. Once the Backplane Type has been determined, it does not preclude the Controller/ Root from using this signal for some other user/vendor specific defined application.~~

~~Part III~~

~~Detailed Description of the change~~

The information contained in this ECR dictates that changes be made to the following tables:

- **Table 3-1: Pinout for Fixed Internal Connectors (root)**
- **Table 3-2: Pinout for Fixed Internal Connectors (end point)**
- **Table 6-9: Wiring Chart for Iternal Passive and Active Crossover Cables**

Relevant changes to the tables listed above are included in the Wiring Chart ECR. For this ECR to be approved, the Wiring Chart ECR must also be approved.